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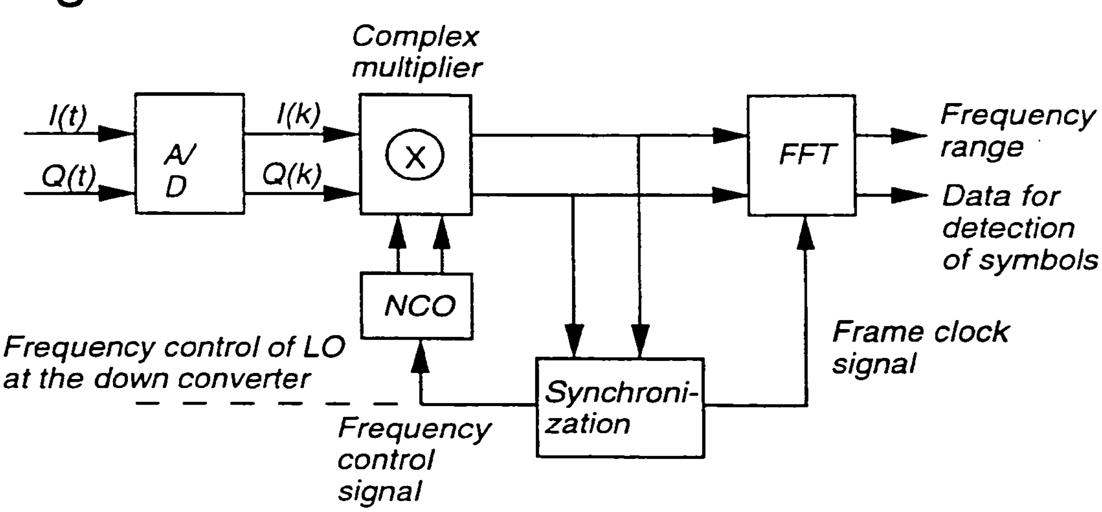
(54) Frequency and frame synchronisation for OFDM

(57) The present invention is a method and device for synchronization at OFDM-systems. A signal is read into the synchronization block in the time domain, i.e. before fourier transforming of the signal via the FFT-processor, according to Figure 1. In the synchronization block the frame clock for start and input of data in the FFT-processor is regained. For OFDM-reception it is very important that this input starts at the right point of time to make possible detection of data. The point of time for the input to the FFT-processor is therefore adjusted in relation to the regained frame clock.

When the frame clock has been regained the frequency error can be estimated, which is also performed in the synchronization block. The frequency error is utilized in a control loop for feed back to an oscillator which generates a complex rotating vector which is multiplied by the input signal for compensation of the frequency error. The invention can be utilized at OFDM-system with guard space or OFDM-system with pulse forming.

Fig.1



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Description

TECHNICAL FIELD

The present invention relates to a system where information is transmitted in orthogonal channels. The information is transmitted in a number of channels. OFDM, Orthogonal Frequency Division Multiplexing, is a transmission method suitable for time dispersive channels. At the present situation OFDM is planned to be used as tranmission method at a large scale within digital sound broadcasting, for instance DAB, HD-TV, high-capacity services on coppar cable, DTM line coding which basically is the same thing as OFDM etc.

PRIOR ART

In the systems which at present are used for synchronization in OFDM-systems a number of multipliers are required. Each multiplier is comparatively expensive, so a minimization of the number of multipliers at the synchronization functions is desirable.

OFDM is implemented among other things as OFDM with guard space, respective OFDM with pulse forming. In OFDM with with guard space a part of the signal interval is detailed for said guard space. In guard space a part of the symbol is repeated. At OFDM with pulse forming the symbols are being pulse formed, which means that the side lobes from each symbol, in the frequency plane, can be supressed which gives a more reliable detection when perfect synchronization can not be guaranteed. This means that one repeats the whole, or a part of the symbol and then multiplies with the pulse form.

In the patent document WO 93/20627 a method and a device is shown which is intended to be used in a digital transmission system. The invention makes use of repetitive synchronization patterns which can be arranged in transmitted data or placed in time slots of their own. The synchronization information is cross correlated with a known value at which the synchronization signal is created by summing up the result from the cross correlation.

In the patent document US 3 883 729 is described av device for frame correlation in a time multiplexed transmission system. The device consists of logical circuits for correlation of an incoming signal with a signal which has been delayed. By that the correlation can be performed on just any signals provided they are repeated.

In the patent document US 5 363 415 is described a "carrying regenerating device" intended for mobile satellite communication. According to the document unique signal sequences are placed periodically among transmitted data. By the cross correlation with known stored sequences, phase- and frequency errors can be calculated.

In document US 4 638 478 synchronization of frames in a TDM-system is described. The synchronization uses circuits which detect guard space. This information is used to secure correct frame synchronization.

The patent document WO 93/11616 describes a digital transmission process which utilizes OFDM. According to ther described process the protection slots are utilized for the transfer of data.

In the patent document US 4 598 413 a circuit arrangement for frame- and phase synchronization of a local sampling clock is described. The synchronization is performed by cross correlation of a received, unique synchronization sequence and one in the receiver stored known sequence.

In the patent document EP 608024 synchronization of an OFDM-receiver is described. A received sequence is correlated with a sequence which is delayed one block length.

In the patent document US 5 148 451 a device for carrier regain in a mobile satellite communications system is described. Unique synchronization words are placed periodically in the transmitted signal. A cross correlation circuit calculates the cross correlation between the received signal and a known stored sequence.

Consequently it is previously known to perform cross correlation of an incoming signal with a locally stored signal. It is also known to utilize a delayed signal where signals exist at certain places in the protocol intended for synchronization. Further the documents show that it is previously known to partially utilize the guard spaces for synchronization.

DESCRIPTION OF THE INVENTION

Technical problem

Simple methods to control time- and frequency errors at OFDM-transmission exist. In the known methods which are used at present there exists a data dependence. Further, known methods require that a number of multiplexings of the signal shall be performed. For each multiplexing a multiplier is required which is comparatively expensive. There is a desire to reduce the number of multipliers to reduce the costs for the synchronization function.

In the known methods, further, special synchronization blocks or synchronization signals are used. The utilization of synchronization blocks or synchronization signals reduces the available space in the signal. In order to effectively utilize the available space it is therefore desirable to find methods where special synchronization blocks or synchroni-

zation signals have been excluded.

The synchronization methods shall further be independent of existing standards and will be produced in different connections for OFDM-system.

The aim with the present invention is to solve the above mentioned problems.

THE SOLUTION

The present invention relates to a method for synchronization of OFDM-systems. An analog signal is digitized in an A/D-converter. The digitized signal is transmitted on a number of channels. The signal is read into a synchronization block. From the synchronization signal the synchronization block determines the position of a frame clock. From the synchronization block a frame clock signal is transmitted to an FFT-block and a frequency control signal to an oscillator. The synchronization of the system is performed before FFT is performed on the signal.

In a further development of the invention the signal includes a symbol and a repeated part of the symbol in the space provided for the signal. The signal is cross correlated at which the repeated part of the signal is given a positive contribution. The cross correlation is calculated by multiplication and sliding mean.

The repeated part of the signal is complex conjugated and multiplied with corresponding part in the signal at which a second signal is created. The second signal is shifted a number of samples corresponding to the repeated part of the signal. The result is subtracted from the second signal and a third signal is created which is integrated and a filtered cross correlation sequence is obtained. The absolute value of the third signal is determined. A saw-tooth signal is obtained which is used for generation of a frame clock by utilizing the peak values of the third signal. The frequency error in the system is determined by calculation of the phase of the cross correlation when the cross correlation has its maximum. The phase shift of the cross correlation is proportional to the length of the symbol.

The invention further relates to a device for synchronization at OFDM-system. A synchronization device is arranged to receive a signal, which signal is digitized and divided into a number of channels. Correlation of the signal is performed by the synchronization device. A synchronization signal is transmitted and the synchronization is performed before the FFT-function. The synchronization device is arranged to transmit a frame clock signal to an FFT-processor. The synchronization device further transmits a frequency signal to an oscillator at which the frequency is adjusted. The signal includes a symbol, L. The symbol is repeated at least to a part in the signal. The repeated signal, R, is preferably placed after the symbol within the signal. The repeated signal, R, is complex conjugated whereafter a multiplication with the corresponding part in the symbol, L, is performed in a multiplying device. A device for sliding mean is arranged to produce synchronization signals from the signal, M, obtained from the multiplication device. The device for sliding mean includes a shift device which is arranged to shift the signal, M, a number of steps corresponding to the length of the repeated signal, R. The result is subtracted from the original signal, M. The obtained signal, C, is integrated in an integrating device. The synchronization device is arranged to calculate the absolute value of the signal, C. A signal, T, including a sequence of triangular signals is produced. The signal generates a frame clock signal to the FFT-processor. The frequency error is determined in the synchronization device by determining the phase shift of the cross correlation. The phase shift is proportional to the frequency error. The frequency error is preferably measured at correlation maxima.

DESCRIPTION OF FIGURES

Figure 1 shows the construction of the invention in the form of a block diagram.

Figure 2 shows the construction of the signal at utilizing of guard space.

Figure 3 shows the construction of the signal at utilizing of pulse forming.

Figure 4 shows synchronization at utilization of guard space.

Figure 5 shows synchronization at utilization of pulse forming.

Figure 6 shows sliding mean filter.

Figure 7 is a detailed picture for sliding mean in the case with guard interval.

Figure 8 shows sliding mean in the case with pulse forming.

Figure 9 shows a sliding cross correlation sequece.

Figure 10 shows the implementation of the synchronization method.

Figure 11 shows the absolute values of cross correlation sequences over six signal intervals for the case OFDM with guard space.

Figure 12 shows a filtered signal in the plane of complex numbers for the case OFDM with guard space.

Figure 13 shows phase variation within a signal interval for the case OFDM with guard interval.

Figure 14 shows the absolute value within a signal interval for the case OFDM with guard interval.

Figure 15 shows the absolute value of a filtered signal for the case OFDM with pulse forming.

Figure 16 shows a filtered signal in the plane of complex numbers for the case OFDM with pulse forming.

Figure 17 shows the phase variations for seven signal intervals for the case OFDM with pulse forming.

DETAILED EMBODIMENT

In OFDM-systems a digital signal is converted in an A/D-converter from analog signal to digital signal. The digital signal is divided into a number of, preferably narrow-band, channels. The digital signal is read into the synchronization block in the time domain, i.e. within fourier transforming of the signal via the FFT-processor according to Figure 1. FFT in this case means Fast Fourier Transform which is described in detail in other literature. In the synchronization block the frame clock is regained for start of the input of data to the FFT-processor. For OFDM-reception it is of outmost importance that this input starts at the right point of time to make possible detection of data. The input point of time to the FFT-processor is therefore adjusted in relation to the regained frame clock.

When the frame clock has been regained the frequency error can be estimated which is also performed in the synchronization block. The frequency error is utilized for a control loop for feedback to an NCO, Numerically Controlled Oscillator, which generates a complex rotating vector which is multiplied by the input signal for compensation of the frequency error. An alternative to this digital control is to control the local oscillators which are utilized for mixing down from radio frequency (the RF-parts are excluded in the Figure). The described synchronization method is focussed on the estimation of frame clock and frequency error. To use these parameters control mechanisms type Phase Lock Loop (PLL) are required, which is required in all types of synchronization methods. The method utilizes that a sufficient part of the information in the OFDM-signal is repeated during each signal interval. This condition is fulfilled in most cases where OFDM is utilized. In the following two main cases are described where this condition is fulfilled:

- OFDM-structure where so called guard space (guard interval) consisting of a repeated cyclical data is utilized.
- OFDM-structure with pulse forming.

In most existing systems based on OFDM, guard space between the symbols are used, see Figure 2. Guard space has as its task to absorb the time dispersion between two following symbols, and to allow delays between a number of audible transmitters (simulcast network). If a 1024 points FFT is utilized, the symbols are sampled 1024 times. The number of samples for guard space can be between zero and a fourth of the FFT-length. Guard space is filled up in the time domain with repeated data, i.e. the first part of the symbol. Because the FFT-operation is cyclic, this causes that the starting point of time for sampling in of symbols can vary within guard space without any information being lost.

There are further variants of OFDM which utilize pulse forming of the symbols. Pulse forming means that the side lobes from each symbol, in the frequency plane, can be suppressed which gives a more reliable detection when perfect synchronization can not be guaranteed.

In the practise this means that one repeats the whole or a part of the symbol and then multiplies by the pulse form.

In Figure 3 the signal interval at utilization of pulse forming is shown. Between two symbols the transition is made "soft" via pulse forming which gives suppressing of side lobes. Henceforth the symbols are however drawn as rectangles for the sake of simplicity.

The main characteristic of pulse forming for this synchronization method is that one utilizes data which is repeated during the signal interval in the transmitted signal.

The synchronization method is based on time continous correlation of samples, time separated bythe repeating distance N. The cross correlation means that during the part of the signal interval which is repeated (correlated), data is given positive contibution. The cross correlation is calculated by multiplication and sliding mean.

In Figure 4 this is illustrated by the length of a symbol being equal to the number of FFT-points. In Figure 4 has been symbolized that a part of the beginning of the symbol L has been repeated in guard space, GS. The repeated signal in guard space. GS, is complex conjugated and multiplied by corresponding part in the original symbol L. The mean value of the result is created and produces a synchronization signal.

In Figure 5 is shown the system at pulse forming. In this case the symbol length consists of the number of FFT-points. In this case half the symbol length is utilized for the symbol and half the symbol length for the repeated function. This means that the same information is repeated in its whole within the symbol length. The repeated symbol is complex conjugated and multiplied by the original signal. The mean value of the result is created and a synchronization signal is transmitted for control of the FFT-block.

The principle for sliding mean is shown i Figure 6. The output signal from the sliding mean is written as C(k) is equal to sum from K equal to minus infinity to infinity.

$$\bar{S}(k)s(k-N) - \bar{S}(k-n)s(k-N-n)$$

$$\bar{S} = \text{complex conjugate}$$

where s(k) is the sampled complex OFDM-signal, N is the repeating distance, and n is the number of sample which is

included in the sliding mean. In the case with guard space, N is equal to the number of FFT-points, and n is equal to the number of samples in guard space. In the case with pulse forming N is the number of FFT-points/two, and n is equal to N.

Synchronization models completed with method for sliding mean are shown in Figure 7 and 8 for the two cases.

The product obtained at the multiplication of the complex conjugated signal and the original signal according to Figure 4 and 5 are read into the shift register in Figure 6. In the shift register the signal is shifted n times. The obtained signal is subtracted from the unshifted signal. The signal which has been obtained in this way is added to a signal which is shifted one step. In this way an integration of the signal is achieved. The result which after that is obtained is a filtered sliding mean cross correlation sequence equal to C(k). In the Figures 7 and 8 the whole process is shown by compilation of the Figures 4 and 6, respective 5 and 6,

In Figure 9 the absolute value of the output signal, C(k), for both variants are shown.

It is important to take the absolute value of C(k), since a frequency error can result in that the signal can be phase shifted which makes C(k) not real.

Filtering of an absolute value calculation gives a saw-tooth shaped signal according to Figure 9 which is very suitable to feed a Phase Lock Loop (PLL) for generation of a frame clock to the following FFT-processor.

The frequency error can easily be calculated from the cross correlation by calculating the phase where the cross correlation has its maximum, as is shown below. Received signal, s'(k) with frequency error can be expressed as

$$s'(k)\, e^{j\omega}\, k \,.\, s(k)$$

where ω is the frequency error. At the cross correlation the following occurs:

$$C(k) = e^{j\omega}\, k \,.\, s(k)\, e^{j\omega}\, (N\text{-}k) \,.\, s(k)\, \bar{s}\, (k\text{-}N)$$

which is simplified to

$$C(k) = e^{j\omega}\, N \,.\, s(k)\, \bar{s}\, (k\text{-}N)$$

Notice that the time dependence, k, has disapppeared from the expression. Consequently the phase shift of the cross correlation is directly proportional to the frequency error ω multiplied by the time distance N. The greater the repeating distance N, the greater the phase shift due to the frequency error, which means that the maximal frequency error which can be detected is:

$$|N^{\omega}| < \Pi \text{ rad.}$$

Or that the frequency error must not exceed:

$$|f_e| < f_s/(2N)$$

where f_e is the frequency error in Hz, and f_s is the sampling frequency in Hz.

The frequency error can, in prinicple, be measured any time within the repeating interval, but to obtain a more reliable estimation this should be done at cross correlation maxima since the phase in that point is based on the mean value of a large number of samples.

A realization model for the synchronization is shown in Figure 8. The sampled complex OFDM-signal is it in two branches. In one branch the sample of the signal N (repeating distance) is delayed in a shift register. The shift register is most easily implemented with FIFO-memories or double gate RAM-memories. The other branch of the signal is complex conjugated. i.e. the imaginary part changes symbol. The two branches are after that multiplied making a complex multiplier.

The output signal from the multiplier is again split into two branches one branch of which is delayed n samples (the number of sample in the sliding mean) in a shift register. The frame clock is regained from the absolute value of the filtered signal at which the function is performed before the PLL-block. There are different ways of simplifying the calculation of the absolute value to avoid further multiplications. A sufficiently good approximation is:

$$\text{aBS}(Z) \approx \max\,(\text{abs}(I), \text{abs}(Q) + 1/2 \text{ times } \min\,(\text{abs}(I), \text{abs}\,(Q))$$

where

$$Z = I + i \cdot Q \text{ (complex notation).}$$

The block "Phase Lock Loop" regains the frame clock, i.e. generates control signal to the FFT-process where it shall start the sampling in of the OFDM-symbol. The block "Phase Detector" has the task to calculate the phase of the correlation sequence at correlation maxima (synchronous with the frame clock). The block "Peak Detector" consequently trigs directly at the frame clock and calculates the phase at this point of time. The phase is at that time directly proportional to the frequency error.

Phase detection shall only be performed once in each signal interval. It is however important that it is performed

at the point of time for correlation maxima, since maximal precision of the phase is given at this point of time. Phase detection can be performed in different ways, for instance by a Pythagoreian processor. look-up table in EPROM, or by a signal processor.

The phase (the frequency error) operates as input signal to a simple feed-back-loop for control of the frequency.

One of the greatest advantages the method presents is the slight complexity which is required by the hardware at the implementation. In the concept is only included:

- one complex multiplier
- two complex adders
- two shift registers
- one phase detector
- logic for calculation of approximized absolute value (compare cell logic and a proper adder)
- logic for PLL (which is included in all synchronization methods)

In Figure 11 the absolute value of a filtered signal is shown. The signal also includes a positive frequency error which is not evident from the absolute value. The Figure shows the result at synchronization of OFDM which contains guard space where the number of FFT-points are 1024 and the number of samples in guard space is 128, and the modulation method QPSK has been utilized. In Figure 12 is shown the filtered signal in the complex number plane for the case OFDM with guard space. If the eight signal intervals in the complex number plane are studied the phase shift due to the frequency error the signal contains will be evident. In Figures 13 and 14 is shown a blow-up of an interval containing a cross correlation maximum. From Figure 13 can be seen how the phase is integrated up to the point where the filtered signal has maximum. The phase detection shall be performed at this point of time to give maximal precision and reliability. Notice that the time scale is identical in Figures 13 and 14.

At synchronization of pulse forms OFDM is in Figure 15 shown the absolute value of a filtered signal. In this case a 1024 points FFT with the modulation method QPSK has been utilized. Figure 11 shows the absolute value of the filtered signal over seven signal intervals. The signal also contains a positive frequency error which can not be seen in the absolute value. If the seven signal intervals in the complex number in Figure 16 is studied, the phase shift due to the frequency error the signal is influenced by will be evident. By a comparison with the guard space case it will be evident that the phase, in principle, is constant within the signal interval. However, maximal precision is given at correlation maxima.

In Figure 17 the phase shift over the seven signal intervals is shown.

The invention is not restricted to what has been described above, but can be subject to modifications within the frame of the patent claims and the description.

Claims

1. Method for synchronization at OFDM-systems, where a digitized signal is divided into a number of channels, and the signal is read into a synchronization block, **characterized** in that the synchronization block from the signal determines the position of a frame clock, that the synchronization block transmits a frame clock signal to an FFT-block and a frequency control signal to an oscillator, and that the synchronization of the system is made before FFT is performed on the signal.

2. Method according to patent claim 1, **characterized** in that the signal includes a symbol and a repeated part of the symbol in the allocated space of the signal.

3. Method according to patent claim 2, **characterized** in that the signal is cross correlated at which the repeated part of the signal is given a positive contribution.

4. Method according to patent claim 3, **characterized** in that the cross correlation is calculated by multiplication and sliding mean.

5. Method according to patent claim 2, **characterized** in that the repeated part of the signal is complex conjugated and multiplied by corresponding part of the signal, at which a second signal is created, which second signal is shifted a number of samples corresponding to the repeated part in the signal, the result of which is subtracted from the second signal and a third signal is created which is integrated and that a filtered cross correlation sequence is obtained.

6. Method according to patent claim 5, **characterized** in that the absolute value of the third signal is determined and that a saw-tooth signal is obtained. which is utilized for generation of the frame clock by utilization of the peak values of the third signal.

7. Method according to patent claim 3, **characterized** in that a frequency error in the system is determined by calculation of the phase of the cross correlation when the cross correlation has its maximum.

8. Method according to patent claim 7, **characterized** in that the phase shift of the cross correlation is proportional to the length of the symbol.

9. Device for synchronization at OFDM-systems where a synchronization device is arranged to receive a signal, which signal is digitized and divided into a number of channels, **characterized** in that a correlation of the signal is performed by the synchronization devices at which a synchronization signal is transmitted, and that the synchronization is performed before an FFT-function.

10. Device according to patent claim 9, **characterized** in that the synchronization device is arranged to transmit a frame clock signal to an FFT-processor.

11. Device according to patent claim 9, **characterized** in that the synchronization device is arranged to transmit a frequency signal to an oscillator, and that the frequency is correlated.

12. Device according to patent claim 9, **characterized** in that the signal includes a symbol (L) and that the symbol at least to a part is repeated in the signal, which repeated signal (R) preferably is placed after the symbol within the signal.

13. Device according to patent claims 9 and 12, **characterized** in that a complex conjugation is performed on the repeated signal (R) whereafter a multiplication by corresponding part in the symbol (L) is performed in a multiplication device, and that a device for sliding mean is arranged to produce the synchronization signal out of the obtained signal (N) from the multiplication.

14. Device according to patent claim 13, **characterized** in that the device for sliding mean includes a shift device which is arranged to shift the signal (N) a number of steps corresponding to the length of the repeated signal (R), the result of which is subtracted from the original signal (N), and that the obtained signal (E) is integrated in an integration device.

15. Device according to patent claims 9 and 14, **characterized** in that the synchronization device is arranged to calculate the absolute value of the signal (C), and that a signal (T) including a sequence of triangular signals is produced, which signal generates the frame clock signal to the FFT-processor.

16. Device according to patent claim 15, **characterized** in that a frequency error is determined in the synchronization device by determining the phase shift of the cross correlation, which phase shift is proportional to the frequency error.

17. Device according to patent claim 16, **characterized** in that the frequency error preferably is measured at correlation maxima.

Fig.1

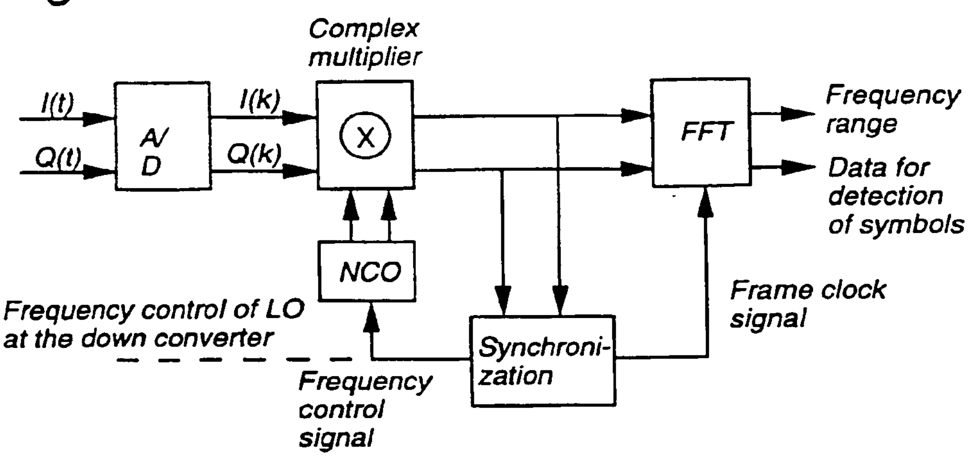


Fig.2

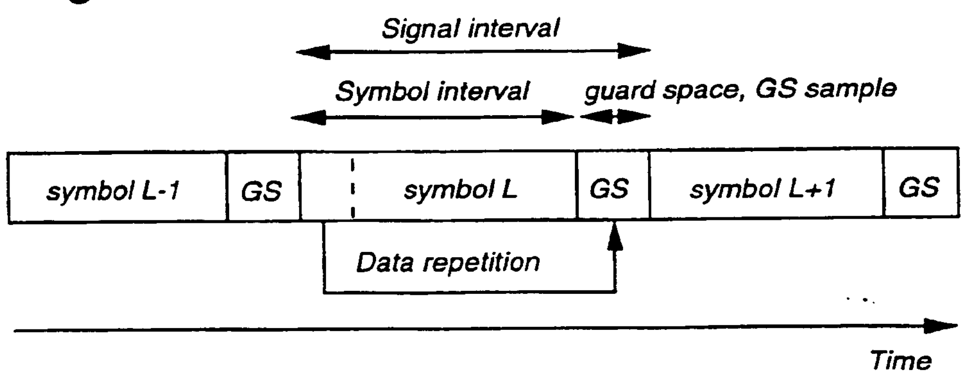


Fig.3

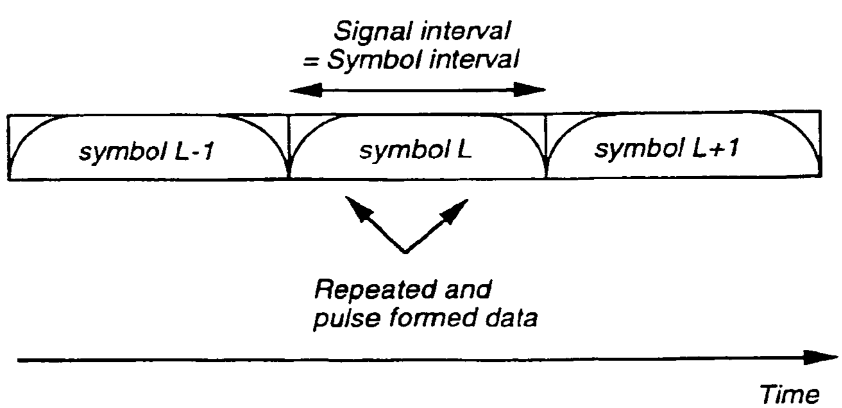


Fig.4

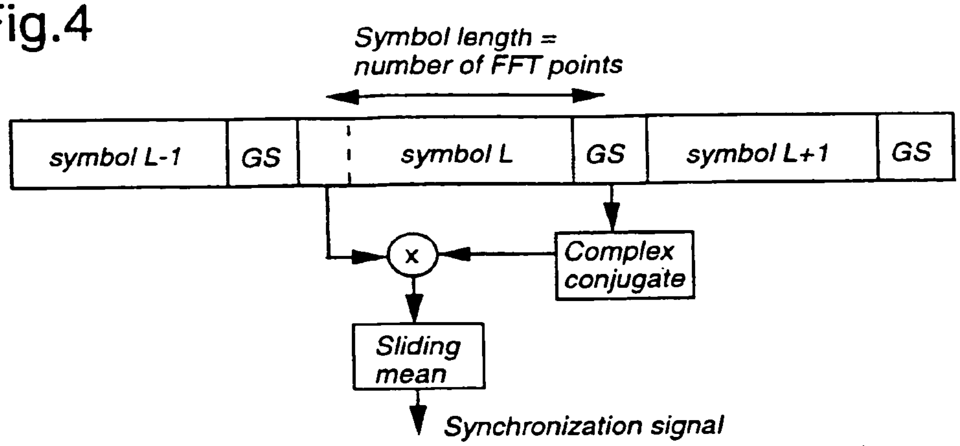


Fig.5

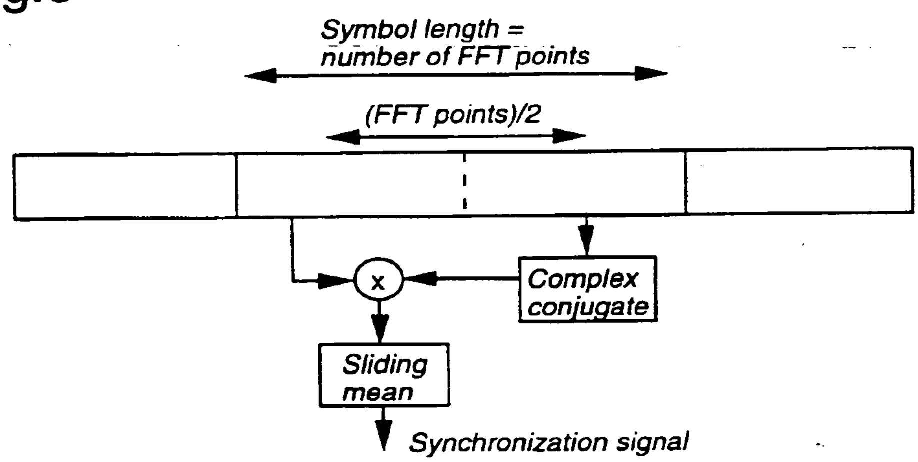


Fig.6

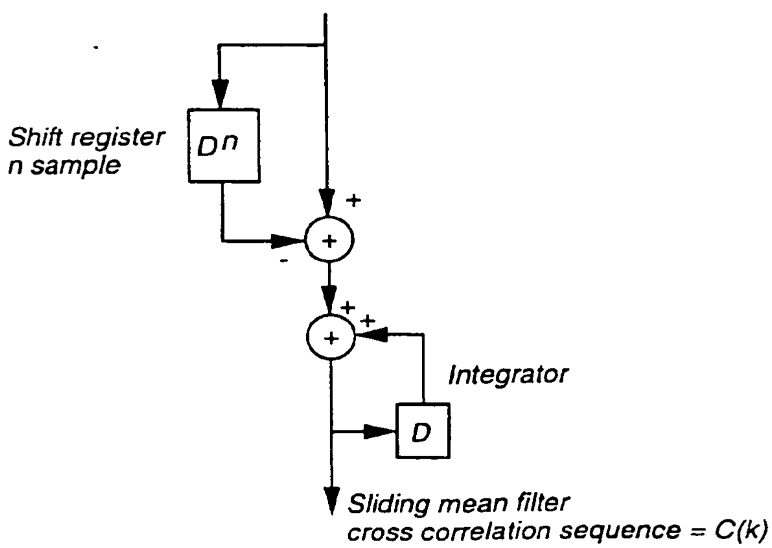


Fig.7

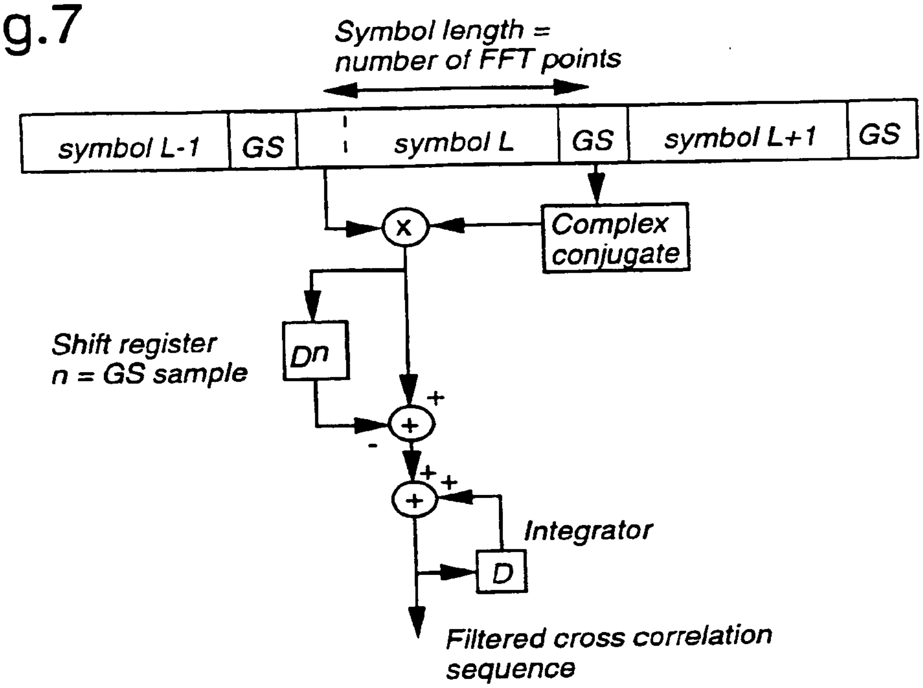

Symbol length =
number of FFT points
symbol L-1
GS
symbol L
GS
symbol L+1
GS
X
Complex
conjugate
Shift register
n = GS sample
Dn
+
-
+
+
+
+
Integrator
D
Filtered cross correlation
sequence

Fig.8

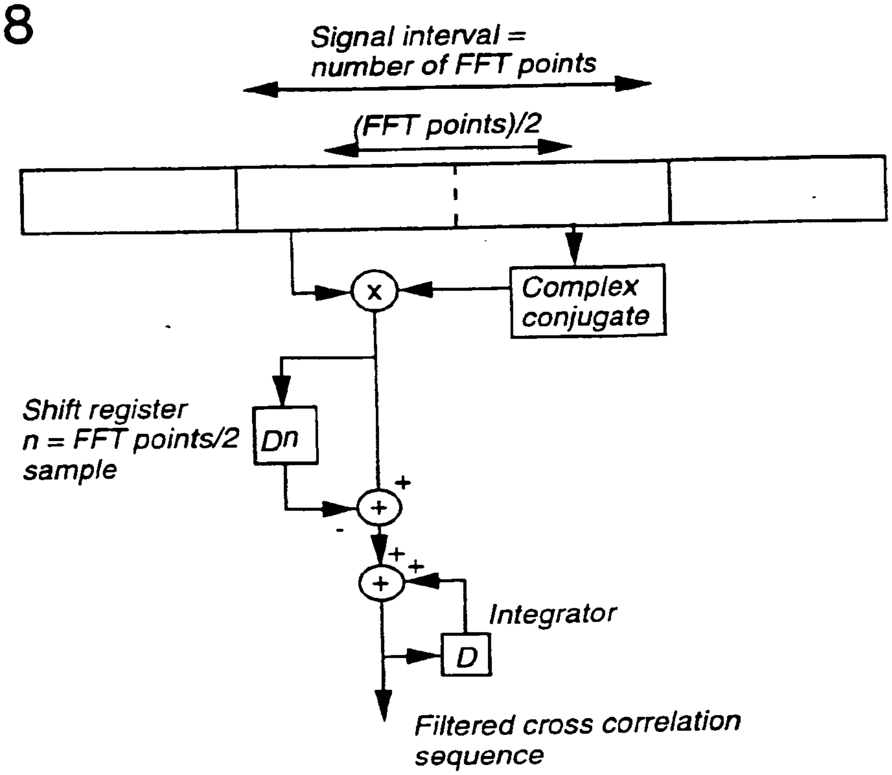

Signal interval =
number of FFT points
(FFT points)/2
X
Complex
conjugate
Shift register
n = FFT points/2
sample
Dn
+
-
+
+
+
+
Integrator
D
Filtered cross correlation
sequence

Fig.9

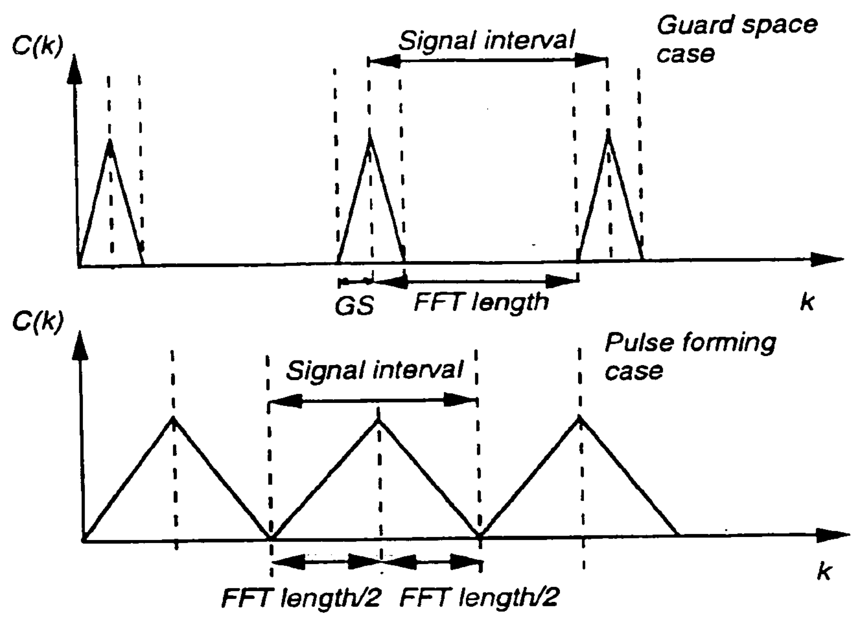

C(k)
Signal interval
Guard space case
GS
FFT length
k
C(k)
Signal interval
Pulse forming case
FFT length/2
FFT length/2
k

Fig.10

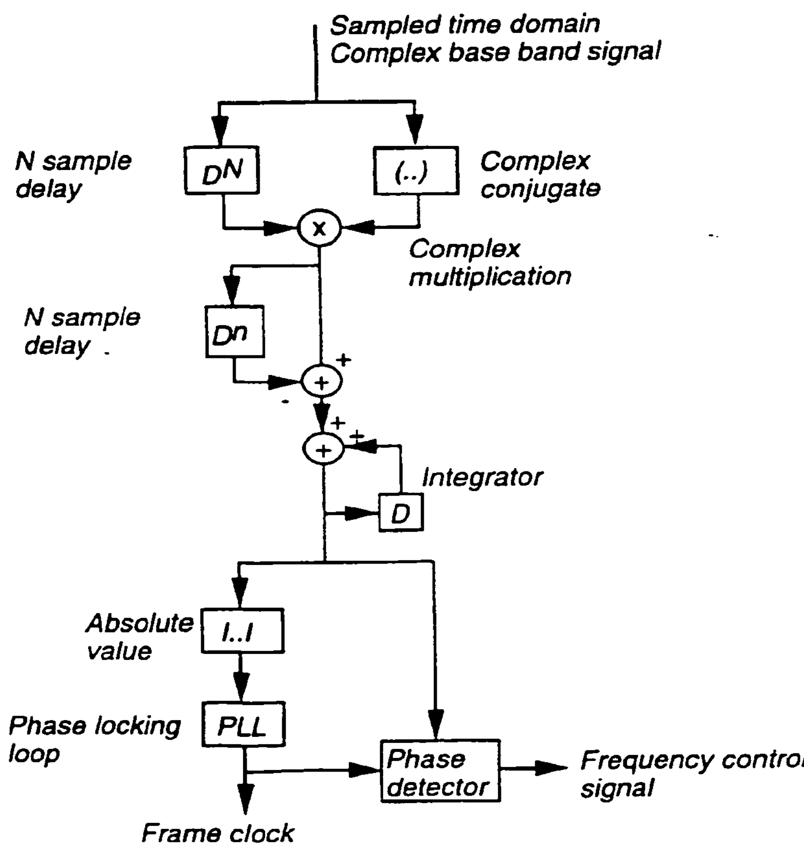

Sampled time domain
Complex base band signal
N sample delay
DN
(..)
Complex conjugate
x
Complex multiplication
N sample delay
Dn
+
-
+
+
+
+
Integrator
D
Absolute value
I..I
Phase locking loop
PLL
Phase detector
Frequency control signal
Frame clock

Fig.11

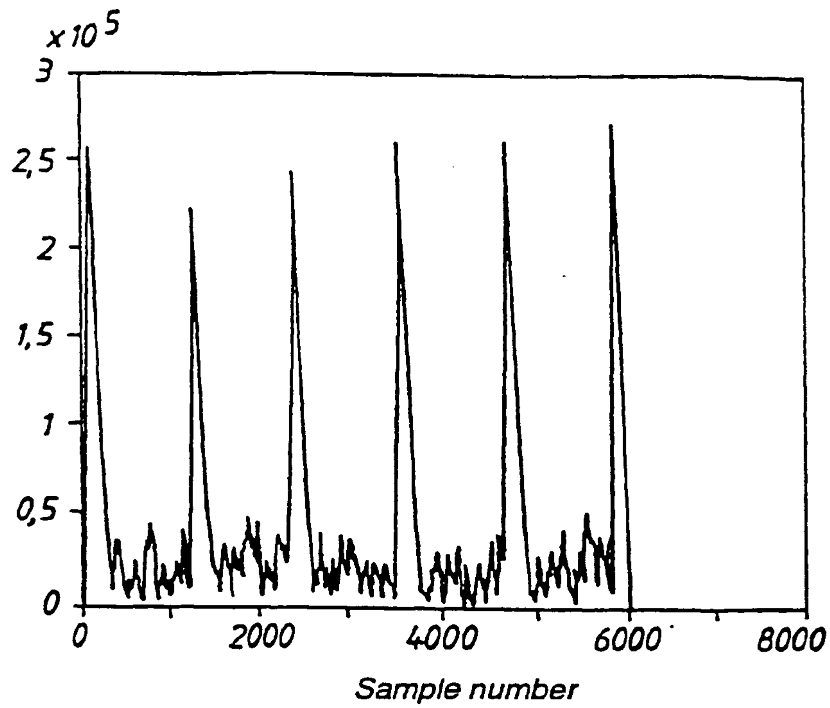

x 10^5
3
2,5
2
1,5
1
0,5
0
0
2000
4000
6000
8000
Sample number

Fig.12

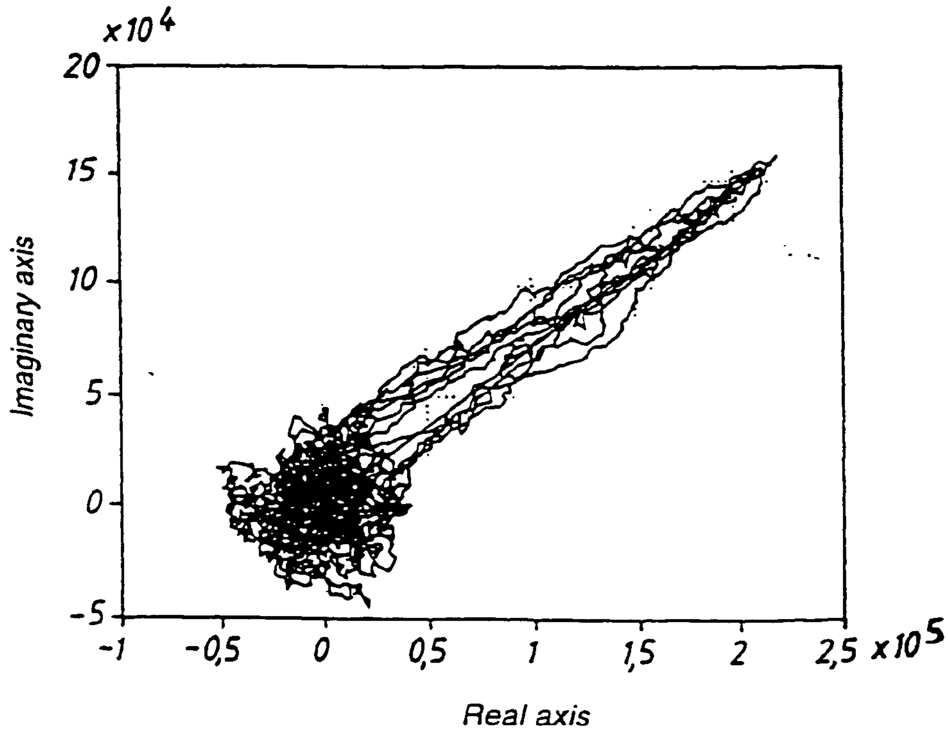

x 10^4
20
15
10
5
0
-5
Imaginary axis
-1
-0,5
0
0,5
1
1,5
2
2,5 x 10^5
Real axis

Fig.13

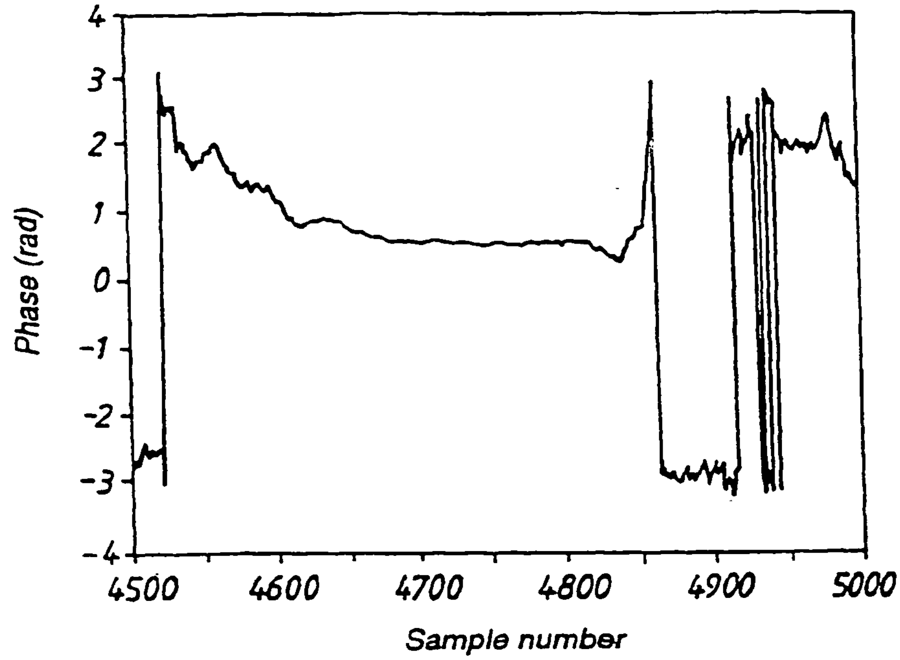

4
3
2
1
0
-1
-2
-3
-4
Phase (rad)
4500
4600
4700
4800
4900
5000
Sample number

Fig.14

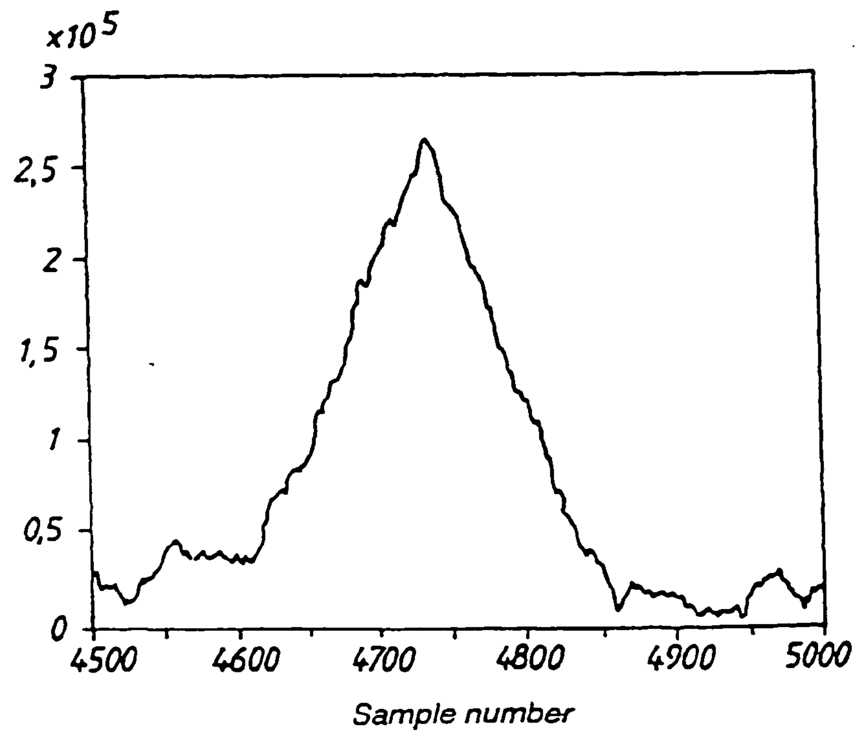

x10^5
3
2,5
2
1,5
1
0,5
0
4500
4600
4700
4800
4900
5000
Sample number

Fig.15

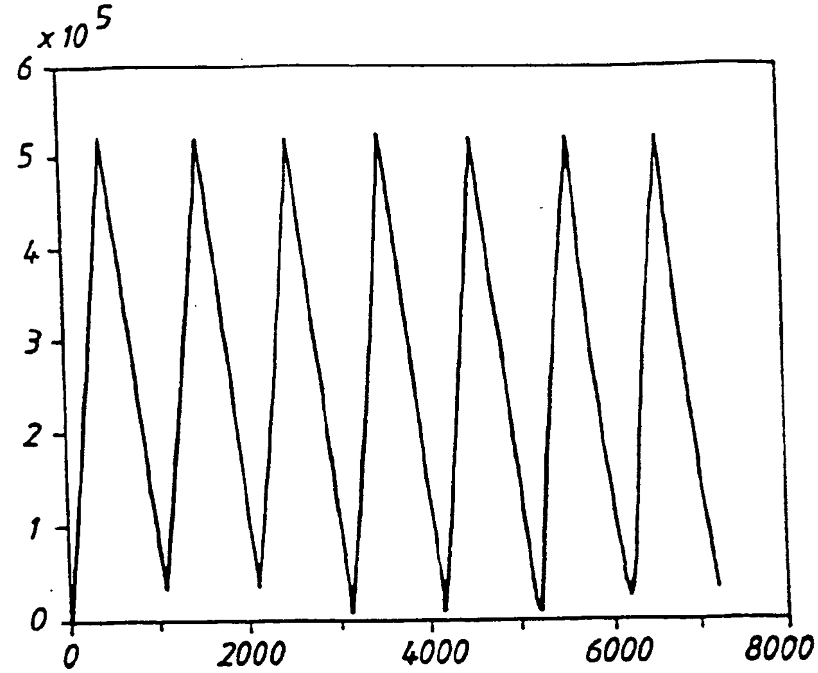

x 10^5
6
5
4
3
2
1
0
0
2000
4000
6000
8000

Fig.16

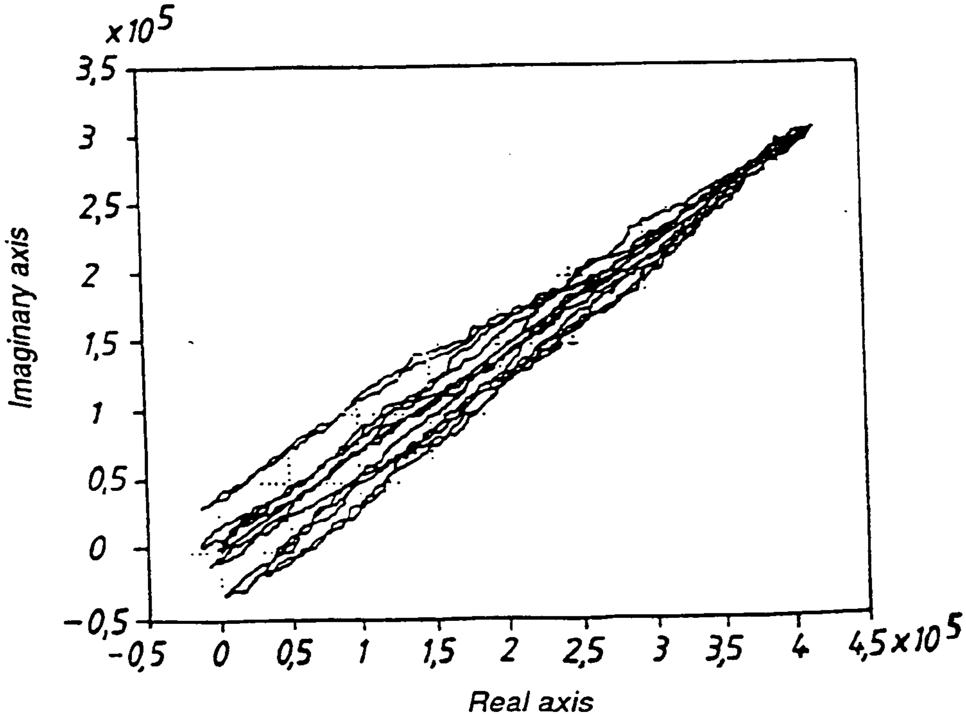
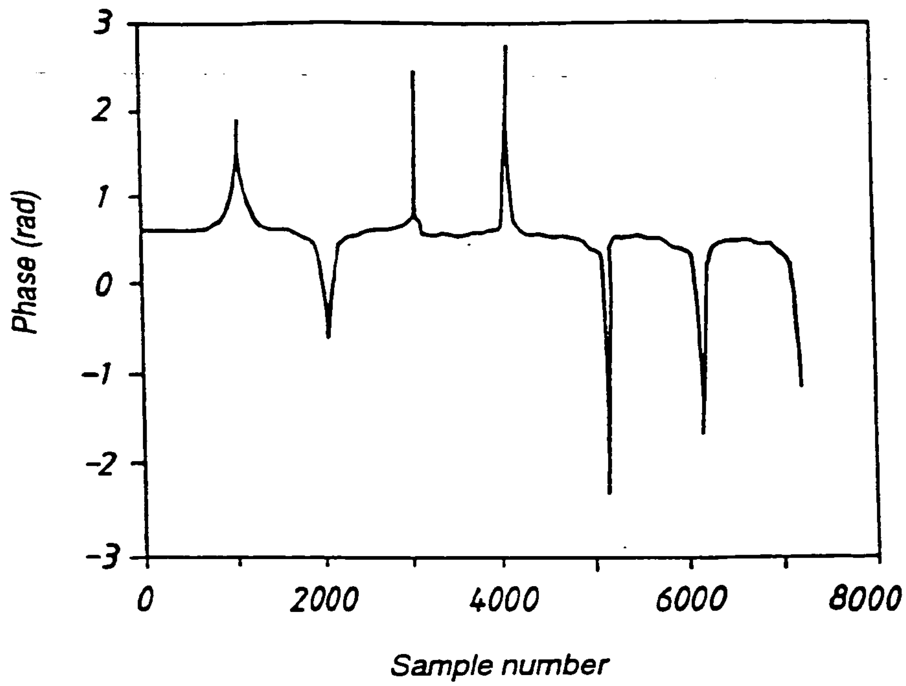

x 10^5
3,5
3
2,5
2
1,5
1
0,5
0
−0,5
Imaginary axis
−0,5
0
0,5
1
1,5
2
2,5
3
3,5
4
4,5 x 10^5
Real axis

Fig.17



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